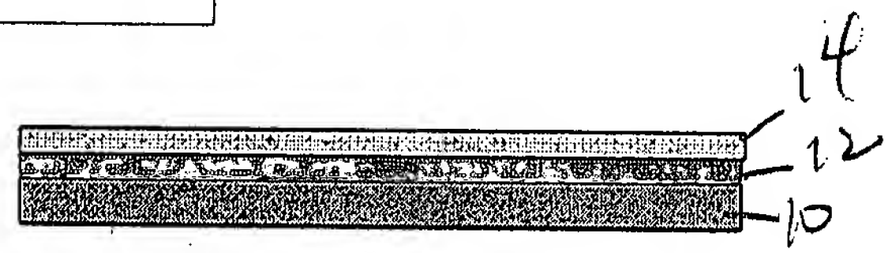
Reverse Neo Process

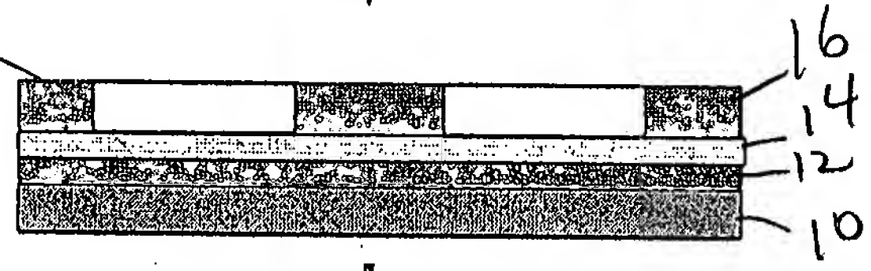
IRVINE SENSORS CORPORATION

Fig. 1c



Photoresist

Fig. 1d



Gold Plating

Fig. 1e

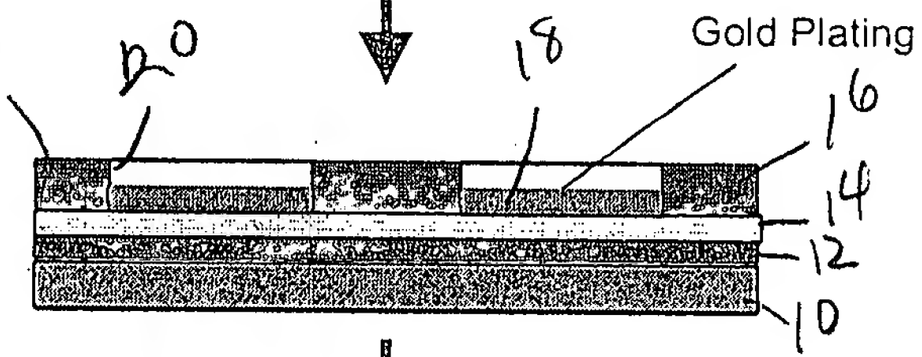
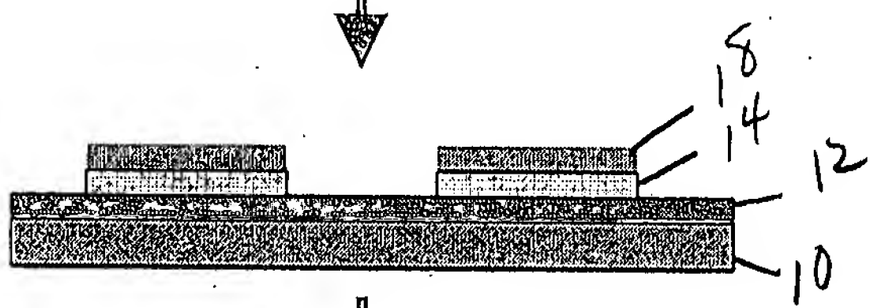


Fig. 1f



1c) Apply field metal

1d) Apply photoresist

1e) Gold electroplate

1f) Strip photoresist & field metal etch

1f

Reverse Neo Process

IRVINE SENSORS CORPORATION

Fig 1g

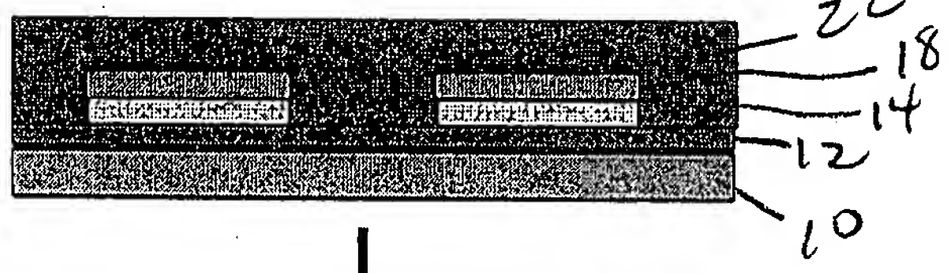


Fig 1h

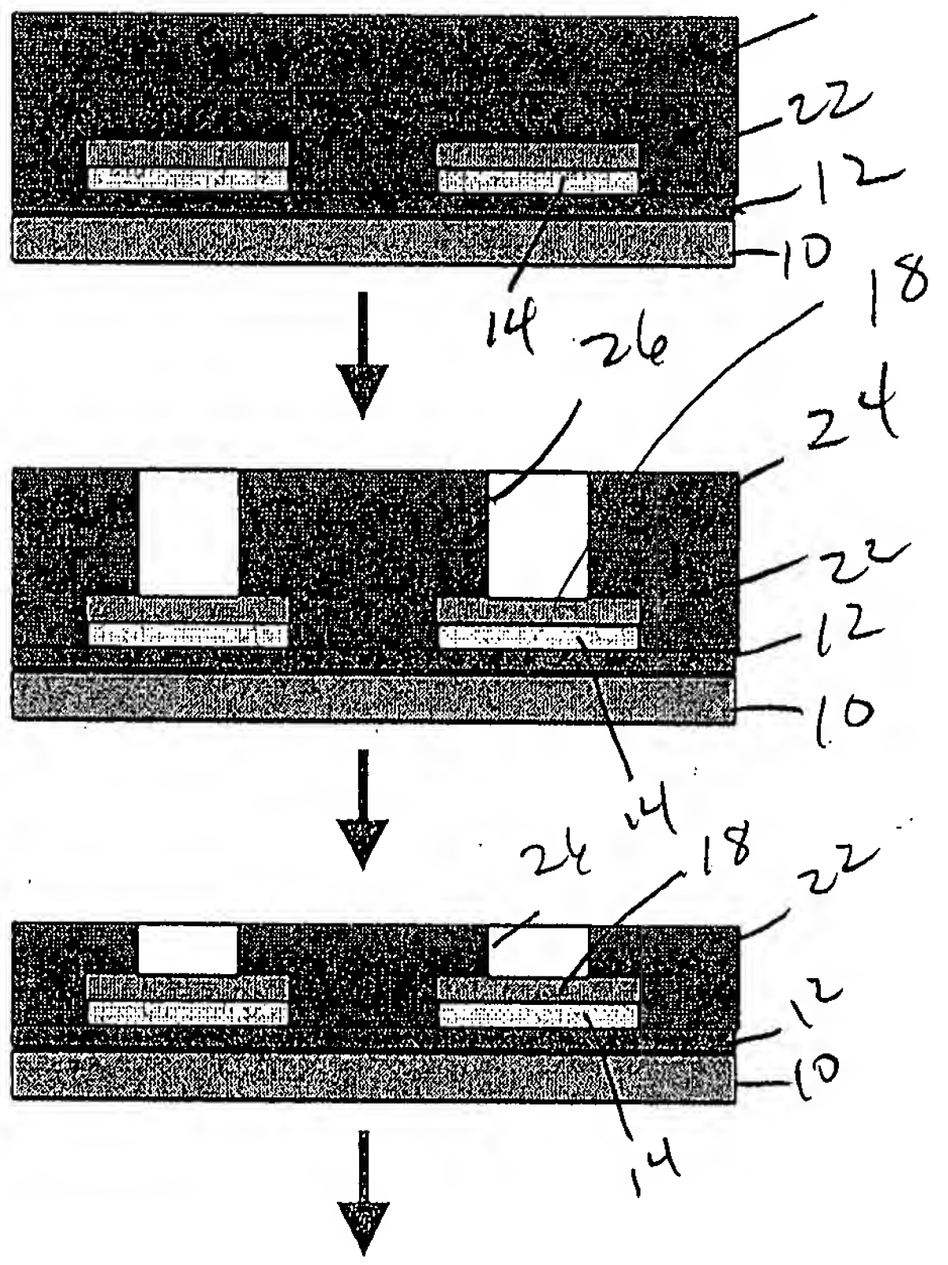


Fig 1i

Fig 1j

1g) Apply polyimide

1h) Apply photoresist

1i) Image & develop photoresist & polyimide

1j) Strip photoresist & cure polyimide

Reverse Neo Process

IRVINE SENSORS CORPORATION

Fig. 1k

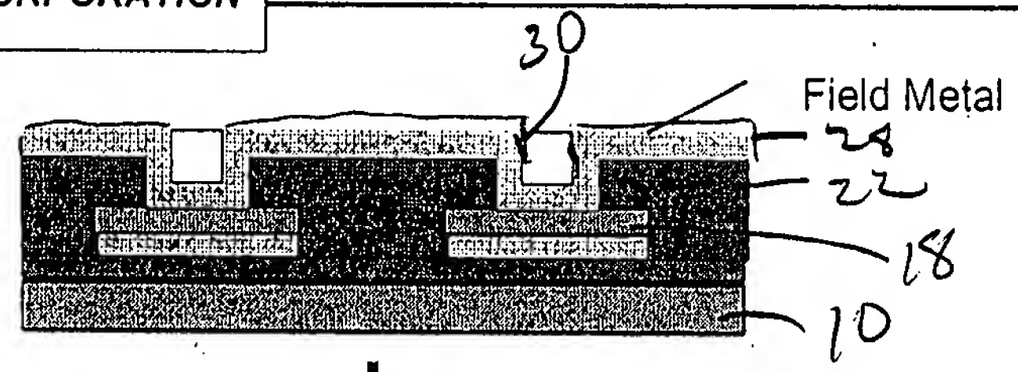


Fig. 1l

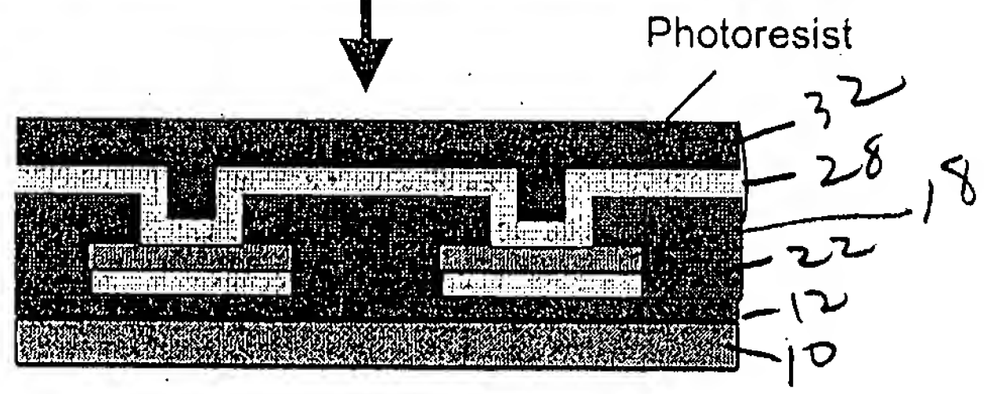


Fig. 1m

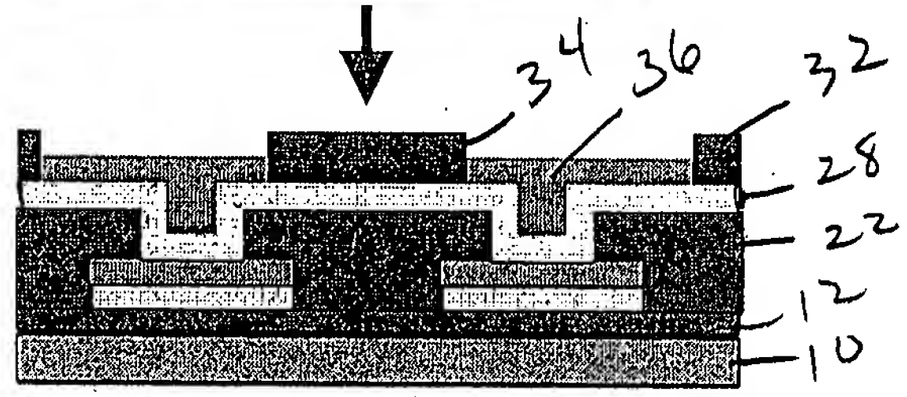
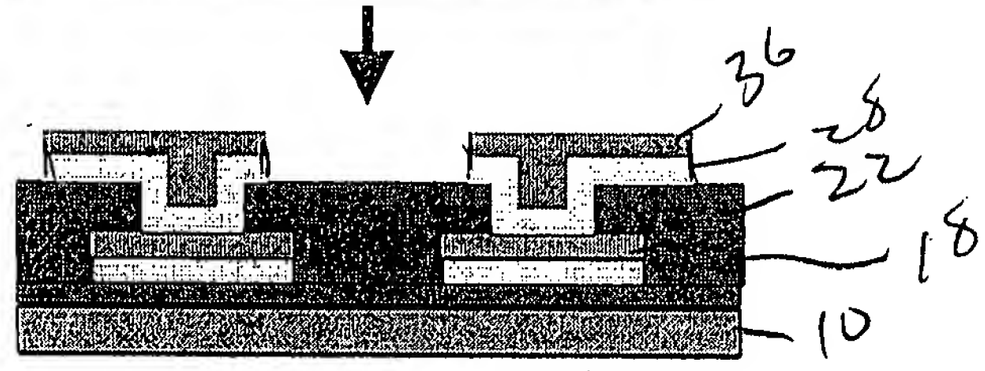


Fig. 1n



1k) Apply field metal

1l) Apply photoresist

1m) Image & develop photoresist. Gold electroplate

1n) Strip photoresist & field metal etch

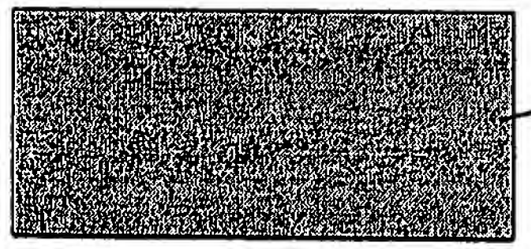
NOTE: For additional layers, steps 1g through 1n are repeated.

Reverse Neo Process

IRVINE SENSORS CORPORATION

Solder Bumping Of Die

Fig 2a



2a) Retrieve die

2b) Apply underbump metalurgy

2c) Apply solder bump

Fig. 2b

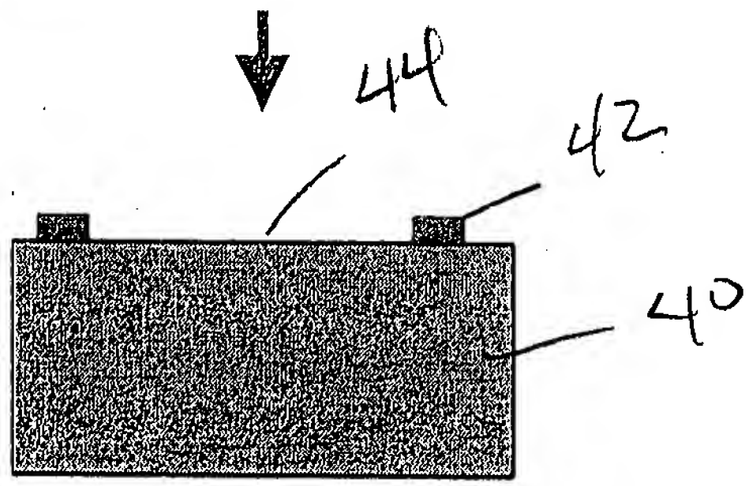
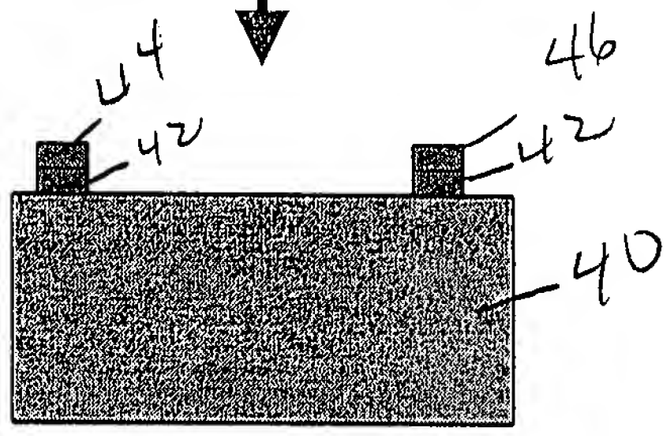
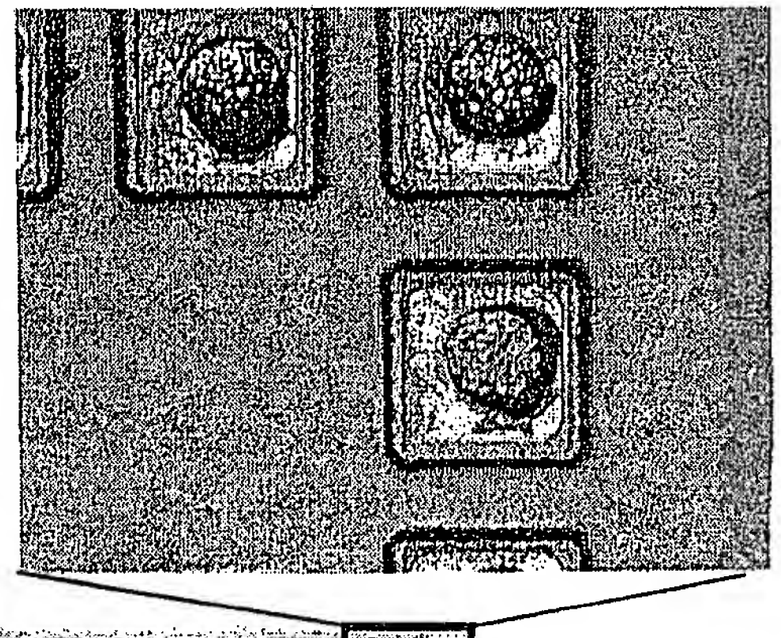
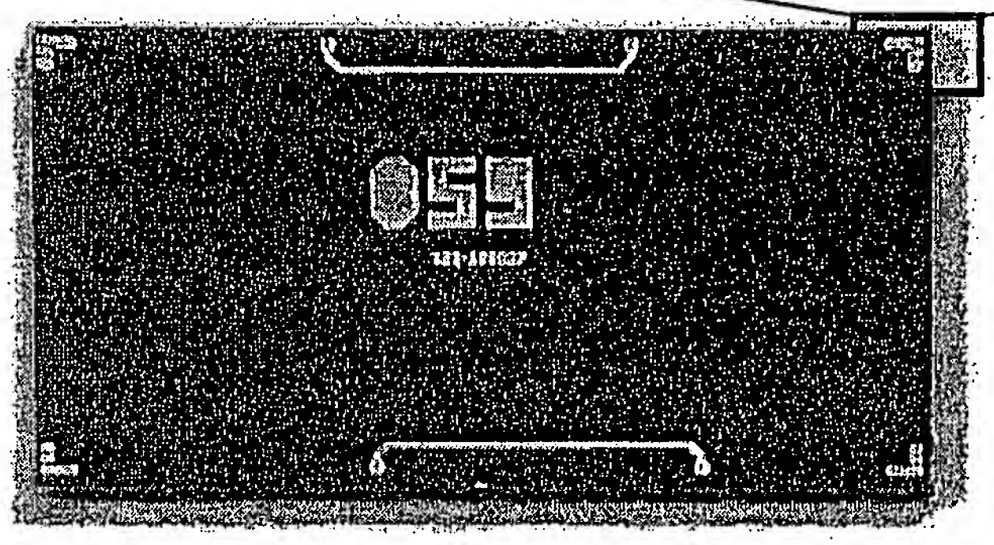


Fig. 2c







2c

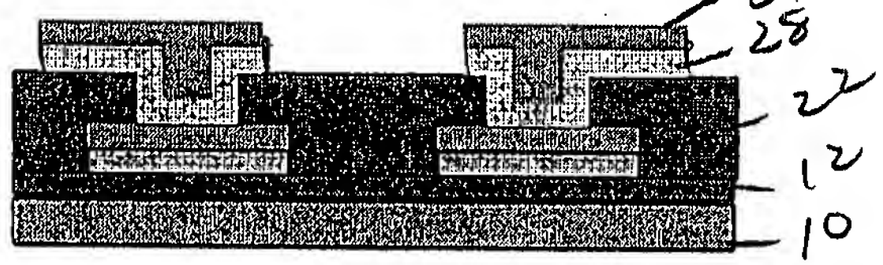
Reverse Neo Process

IRVINE SENSORS CORPORATION

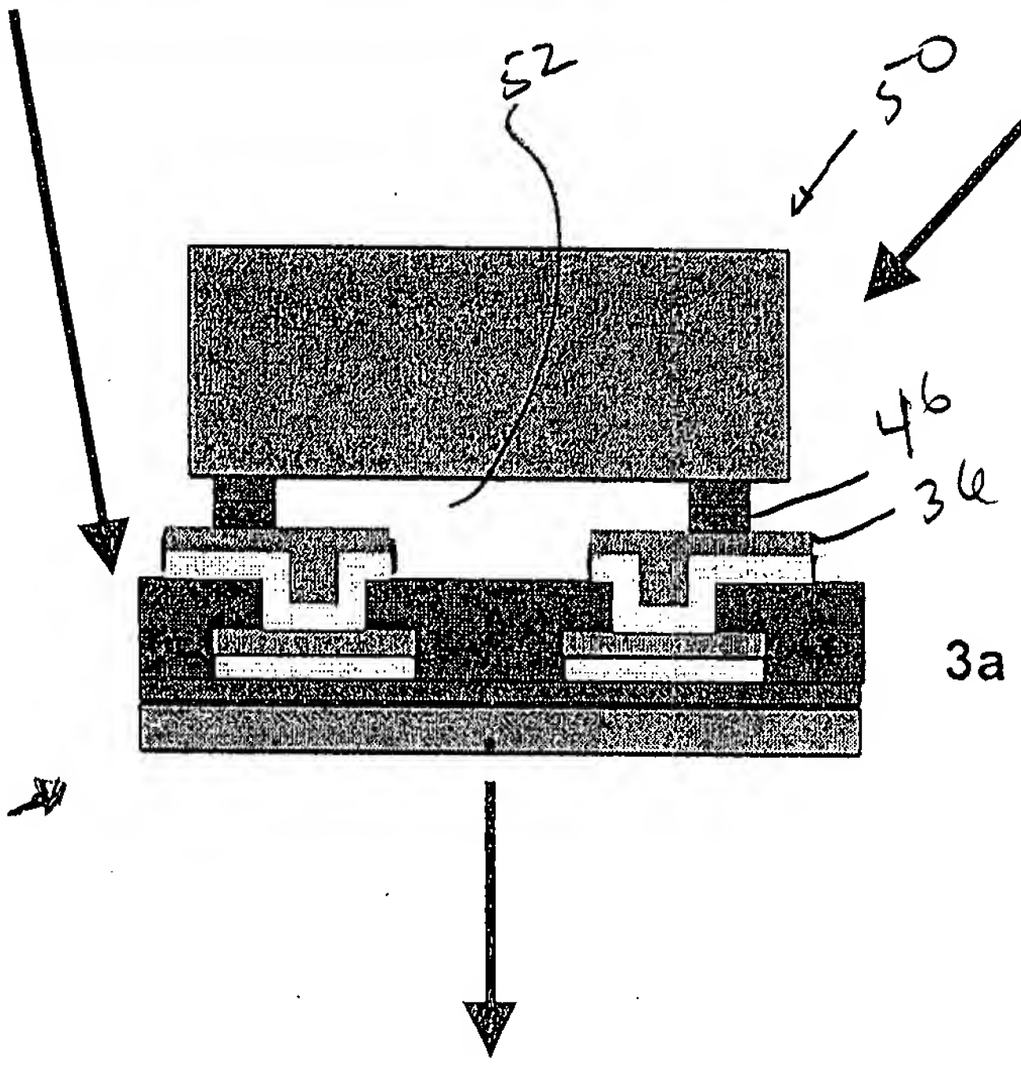
Flip-Chip Bonding

Fig. 3a

1n

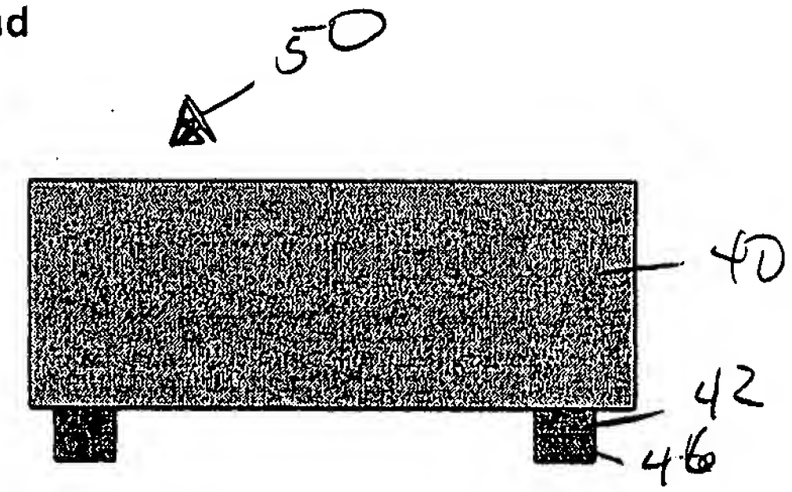


48

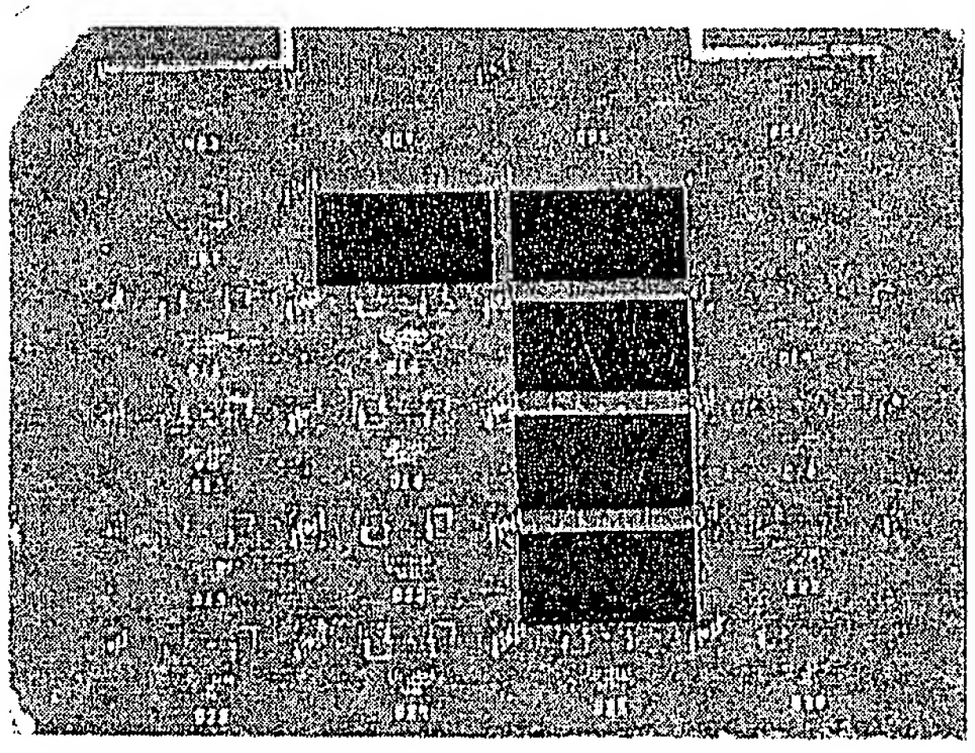


Retrieve substrate assembly and bumped die

2c



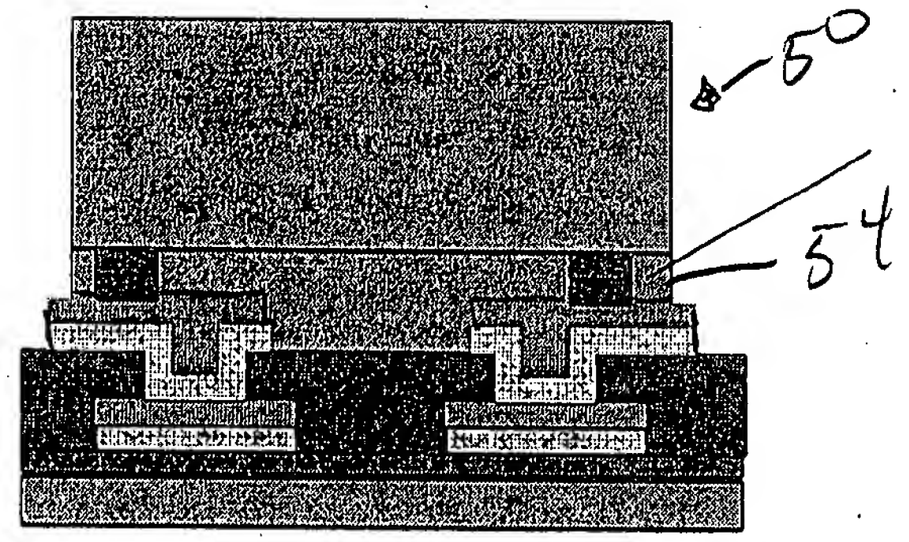
3a) Flip chip bumped die to substrate



Reverse Neo Process

IRVINE SENSORS CORPORATION

Fig 3b



Under fill die

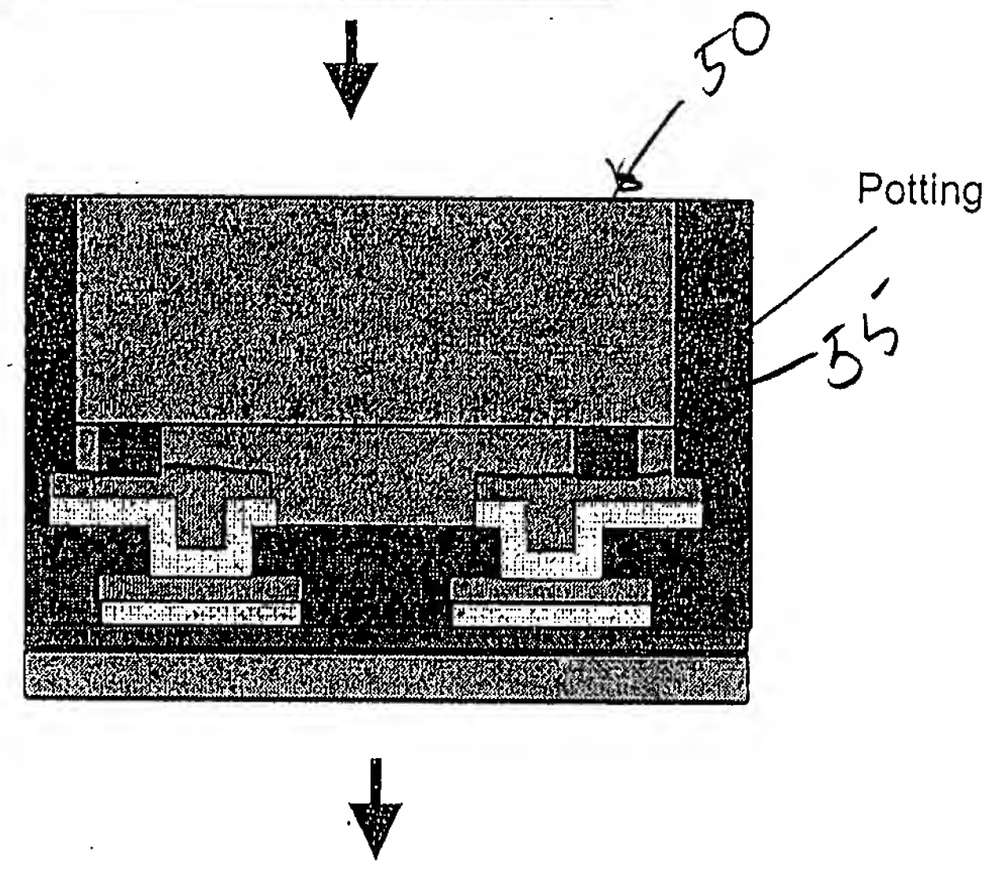


Fig 3c

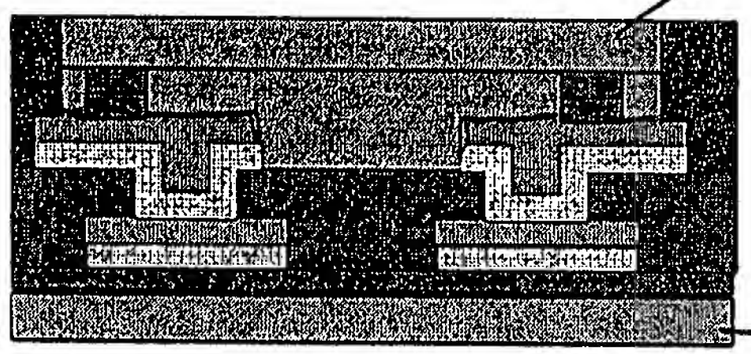
3b) Underfill die

3c) Pot die

Reverse Neo Process

IRVINE SENSORS CORPORATION

Fig. 3d



3d) Thin wafer

3e) Release wafer from aluminum substrate

3f) Mask wafer for test pad etch

Fig 3e

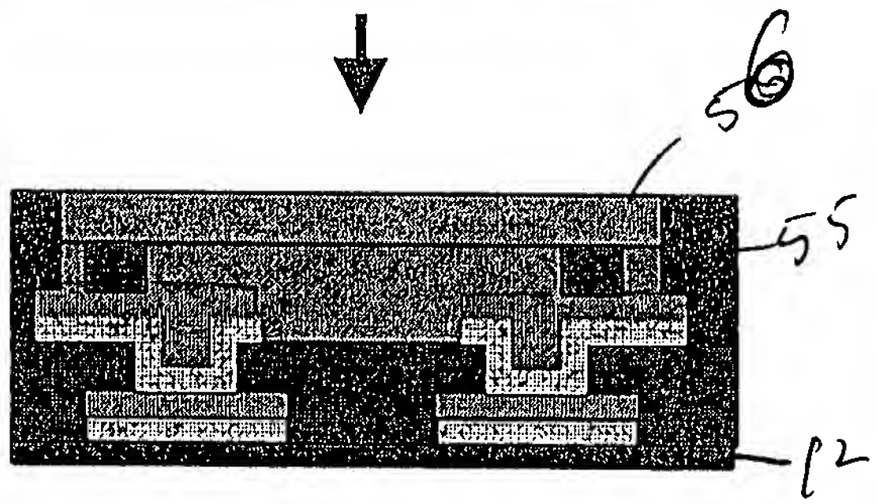
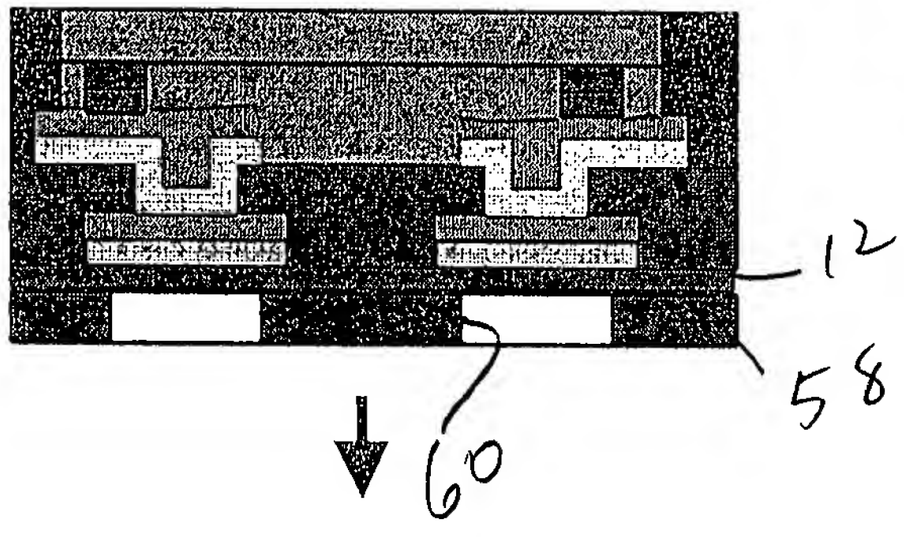
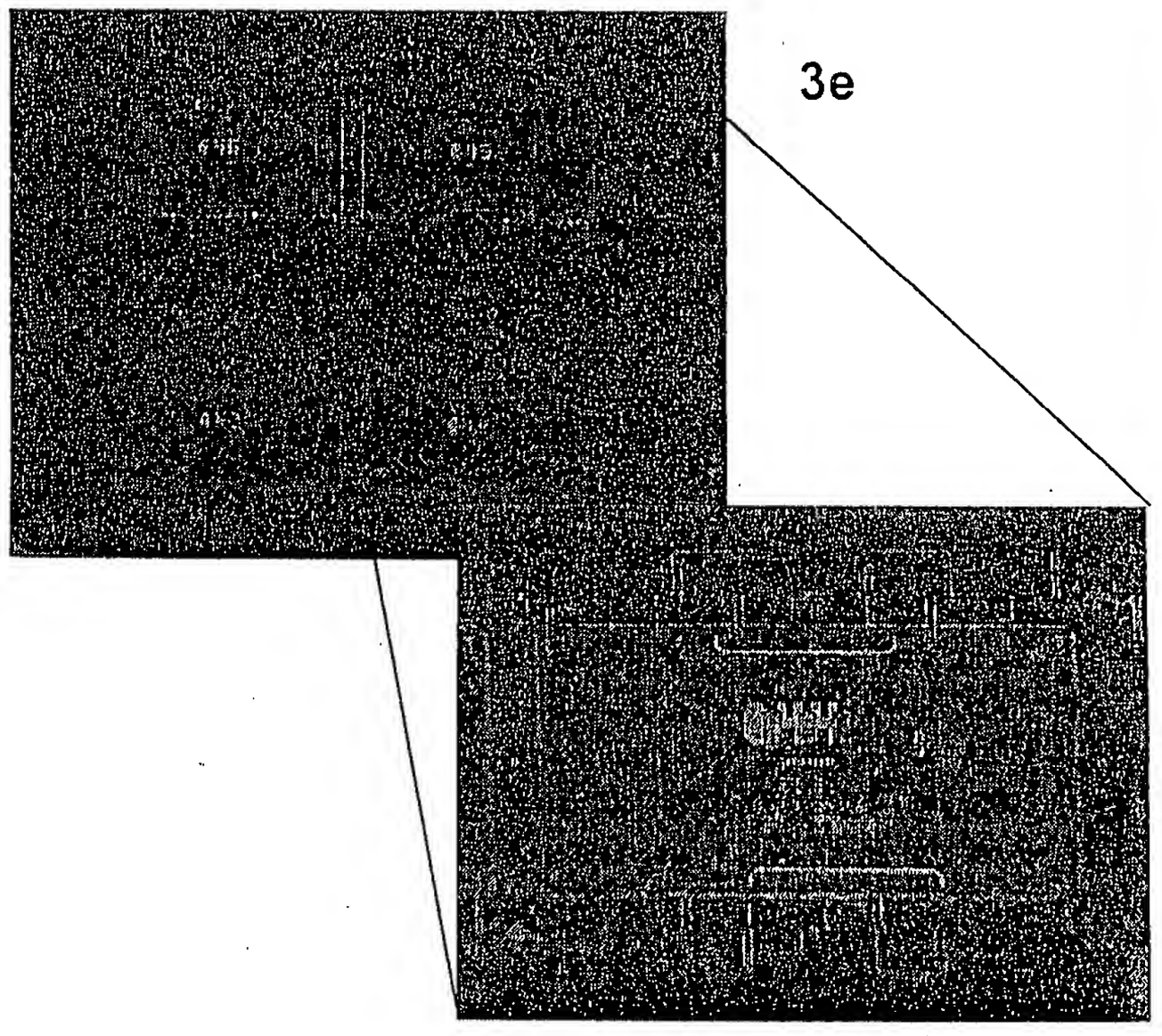


Fig 3f





Reverse Neo Process

IRVINE SENSORS CORPORATION

Fig 3g

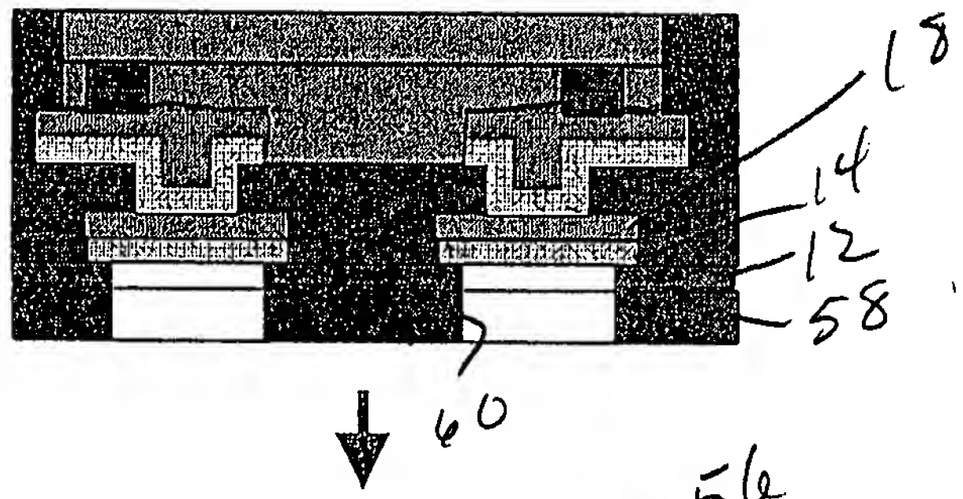


Fig 3h

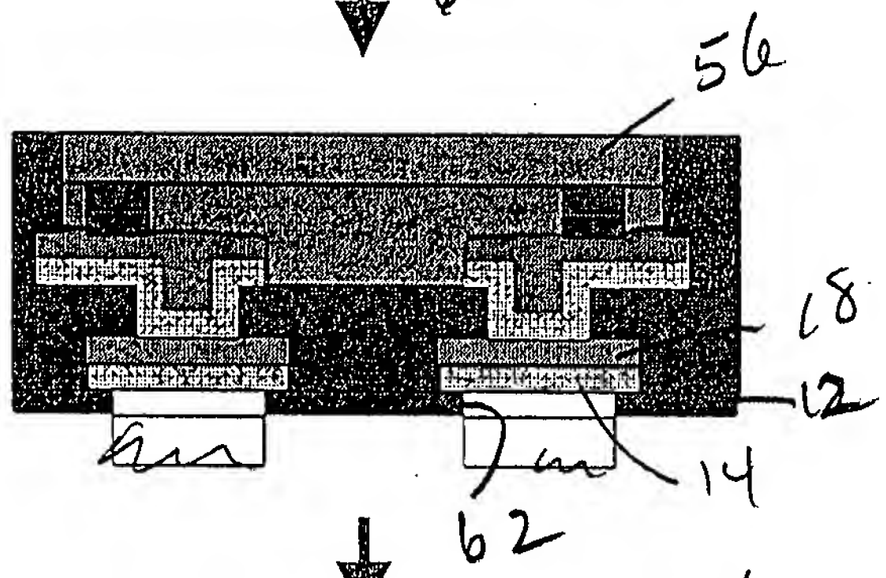
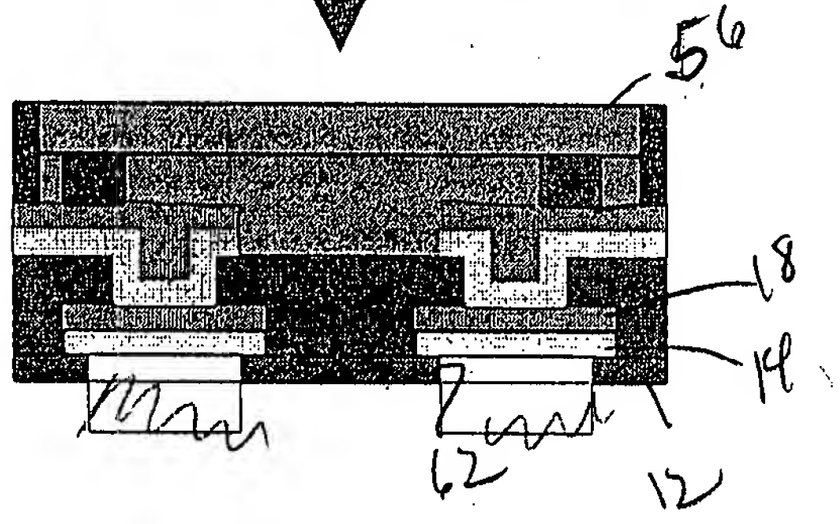


Fig 3i



3g) Etch polyimide to expose test pads

3h) Remove etch mask & test wafer

3i) Dice wafer

High Volume Reverse NEO Process

#1) Wafer Built Up Assembly

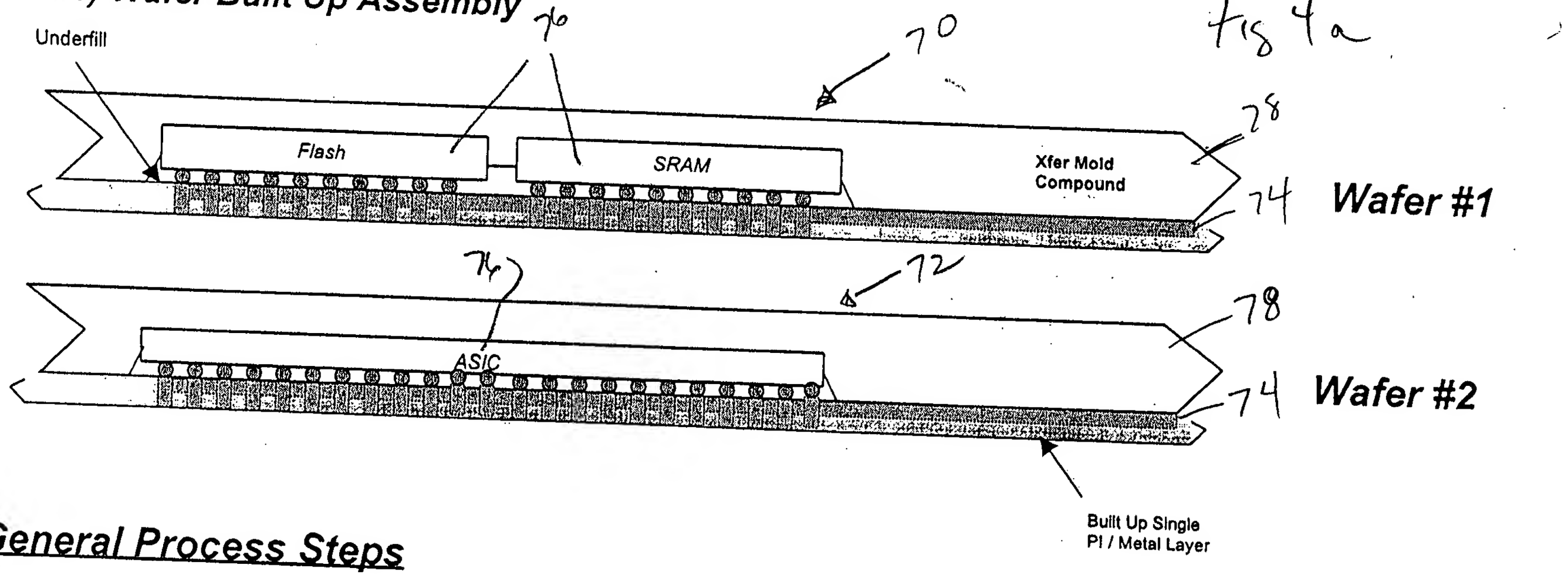


Fig 4a

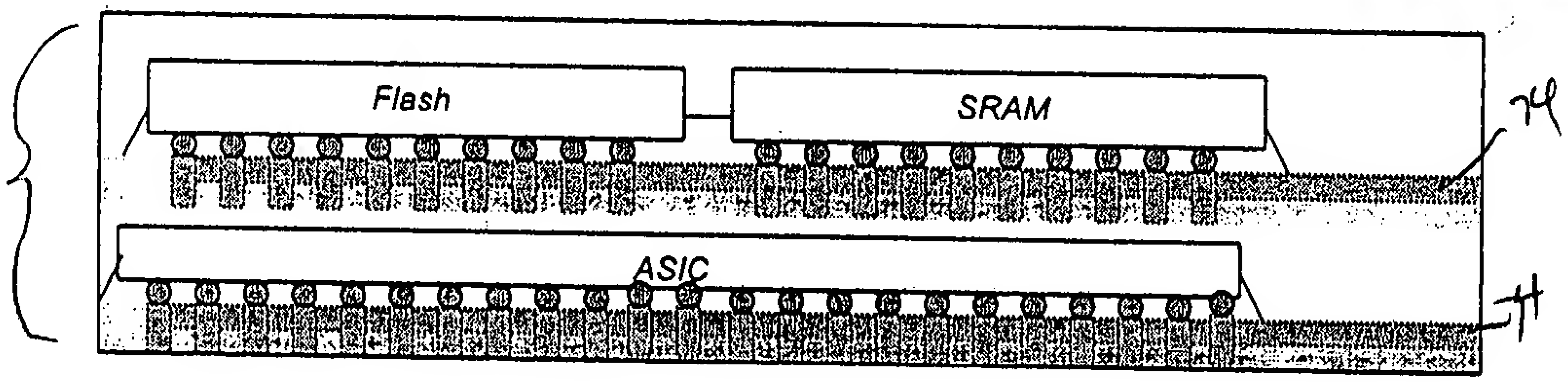
General Process Steps

1) Screen Print Electrically Conductive Epoxy on Built-Up Laminate Substrates
2) Place Flip Chip Devices
3) Cure Epoxy
4) Underfill Devices
5) Xfer. Mold Devices

High Volume Reverse NEO Process

Fig. 4b

2) Stacked Wafer Strip Assembly

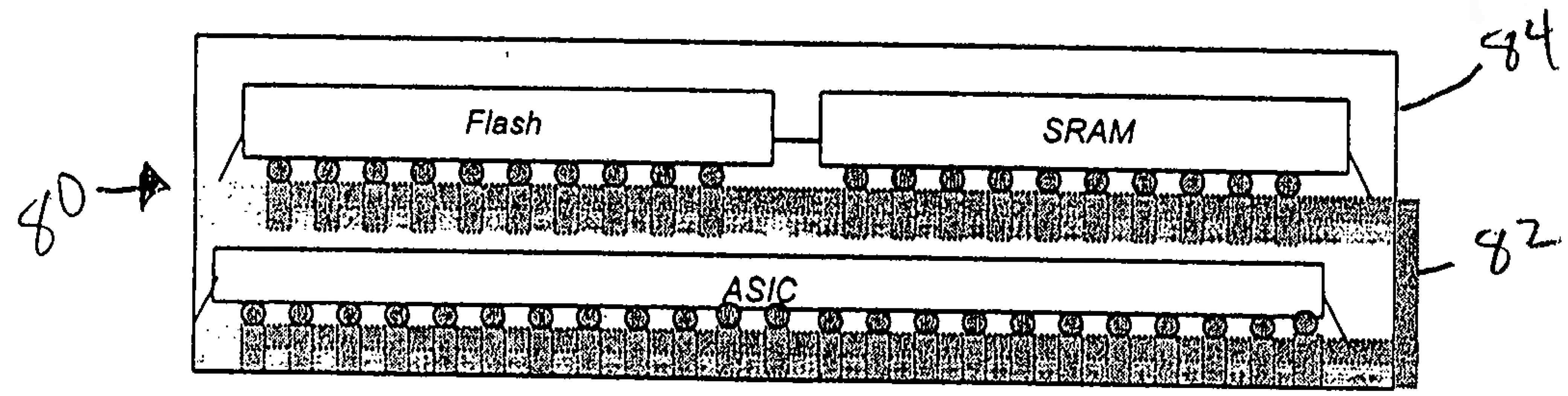


General Process Steps

6) Release Carrier Film from Substrate (If Required)
7) Attach Memory and ASIC Wafers
8) Cut/Saw Wafers to Strips

Fig. 4c

3) Stacked Wafer Strip Assembly



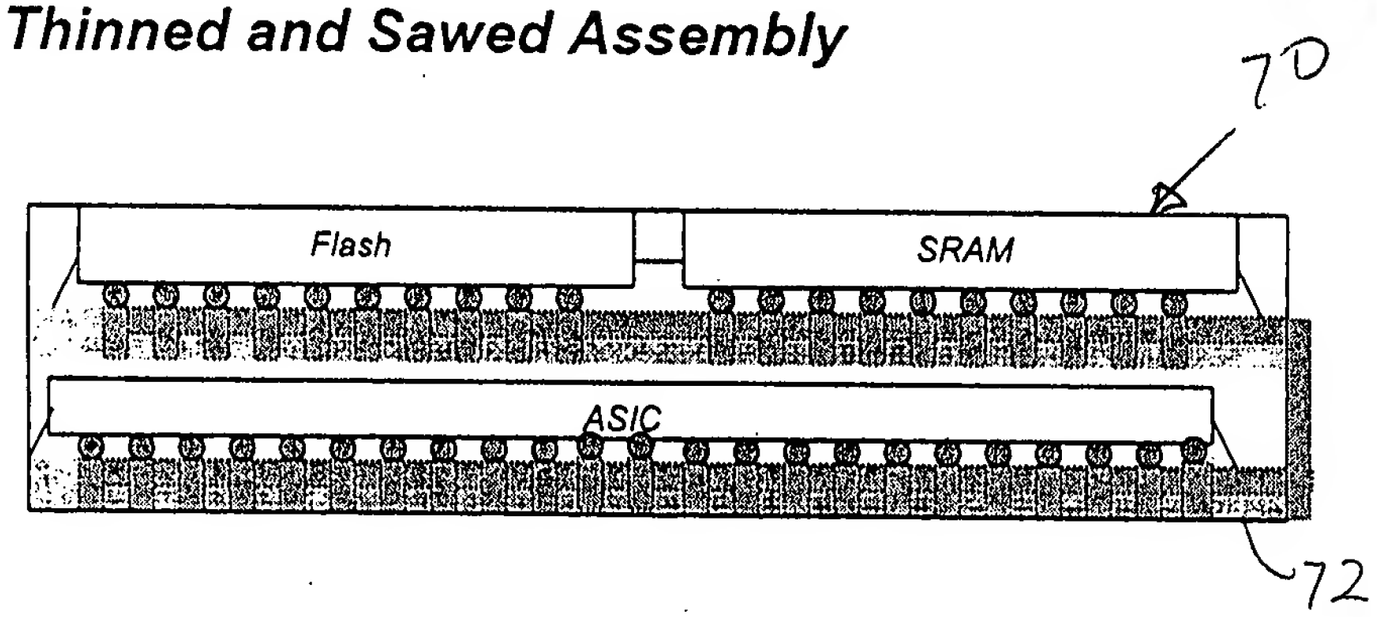
General Process Steps

9) Interconnect or Bus Wafers by Metallizing Wafer Stacks

High Volume Reverse NEO Process

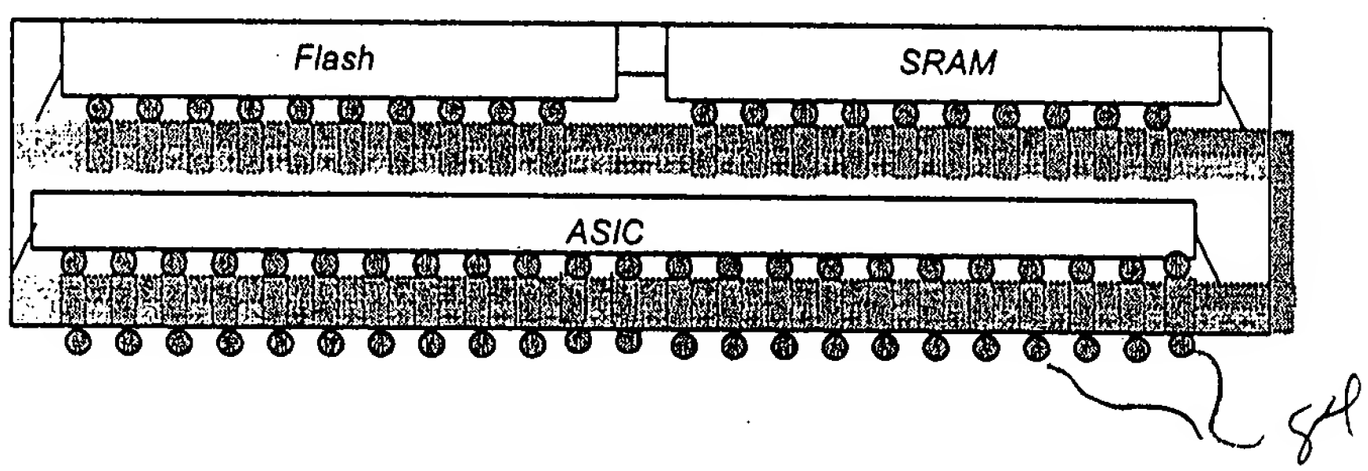
4) Thinned and Sawed Assembly

Fig. 4d



5) Thinned and Sawed Assembly

Fig. 4e



General Process Steps

10) Thin Stack Assembly

General Process Steps

11) Solder Bump Stack
12) Singulate (Saw) into Individual Stacks